## REMARKS

In order to advance the prosecution, a substitute specification has been submitted, the substitute specification has been editorially amended to conform the specification to U.S. patent practice. No new matter has been added. Additionally, claims 1, 7 and 12 have been amended to particularly point out and distinctly claim the invention. Claims 1-18 are pending in the application.

In view of the foregoing amendments and remarks, an early action on the merits is requested. If the Examiner believes that a conference would be of value in expediting the prosecution of this application, the Examiner is invited to telephone the undersigned to arrange for such a conference.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment and a substitute specification is attached in clean form as well as a marked up version. The attached page is captioned "**Version with markings to show changes made**".

Respectfully submitted,
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**Version with markings to show changes made**

**In the Title**:

Please amend the title as follows:

--SEMICONDUCTOR MEMORY DEVICE HAVING A PLUG CONTACTED TO A CAPACITOR ELECTRODE AND METHOD FOR FABRICATING THE [SAME] CAPACITOR--

**In the Specification**:

Attached hereto is a substitute specification in clean form and a marked up version. It is respectfully submitted that the substitute specification is in compliance with 37 CFR §1.125(b) and no new matter has been added.

**In the Claims**:

Please amend claims 1, 7 and 12 as follows:

1. (Amended) A semiconductor memory device, comprising:

a semiconductor substrate, [wherein] a gate electrode [is] formed on the semiconductor substrate, and [wherein] a plurality of source/drain junctions [are] formed in the semiconductor substrate;

an interlayer insulating layer formed over the semiconductor substrate;

a plug formed in the interlayer insulating layer, [wherein] the plug [comprises] includes a diffusion barrier layer and a

seed layer for [a] electro plating;

a lower electrode of a capacitor contacted to the seed layer;

a dielectric layer formed on the lower electrode; and

an upper electrode formed on the dielectric layer.

7. (Amended) A method for fabricating semiconductor memory device, comprising the steps of:

providing a semiconductor substrate, [wherein] forming a gate electrode [is formed] on the semiconductor substrate, and [wherein] forming a plurality of source/drain junctions [are formed] in the semiconductor substrate;

forming an interlayer insulating layer over the semiconductor substrate;

etching the interlayer insulating layer [to form] and forming a contact hole;

forming a plug in the contact hole, wherein the plug [comprises] includes a diffusion barrier layer and a seed layer for [a] electro plating;

forming a lower electrode of a capacitor contacted to the seed layer by using an electro plating technique;

forming a dielectric layer of the capacitor on the lower electrode; and

forming an upper electrode of the capacitor on the dielectric layer.

12. (Amended) A method for fabricating semiconductor memory device, comprising the steps of:

providing a semiconductor substrate, [wherein] forming a gate electrode [is formed] on the semiconductor substrate, and [wherein] forming a plurality of source/drain junctions [are formed] in the semiconductor substrate;

forming an interlayer insulating layer over the semiconductor substrate;

etching the interlayer insulating layer [to form] and forming a contact hole;

forming a plug in the contact hole, wherein the plug [comprises] includes a diffusion barrier layer and a seed layer for [a] electro plating;

forming a glue layer on the seed layer and the interlayer insulating layer;

forming a sacrificial layer on glue layer;

etching the sacrificial layer and the glue layer [to form] and forming an opening defining a region of a lower electrode of a capacitor;

forming the lower electrode on the seed layer in the

opening, by using an electro plating technique;

removing the sacrificial layer and the glue layer;

forming a dielectric layer of the capacitor on the lower electrode; and

forming an upper electrode of the capacitor on the dielectric layer.